Abstract of the Disclosure

A data memory cache unit is provided which is capable of heightening the speed of memory access. The cache unit 117 executes reading and writing of data in a 16-byte width line unit in a main memory unit 131, executes reading and writing of data in an MPU 113 in the unit of a four-byte width small area included in each line. When the MPU 113 executes a push instruction, if a cache miss takes place on a line which includes a small area that holds data which should be read out to the MPU 113 (NO at S1), then the cache unit 117 opens the line (S301). If a small area into which the data sent from the MPU 113 should be written is adjacent to a line boundary on the side where an address is larger or on the side where write-in is earlier executed (YES at S56), then the cache unit 117 does not execute a refill, and if this small area is not adjacent to the line boundary (NO at S56), then it executes a refill (S21).